R09

Code No: D7702, D5702

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II - Semester Examinations, March/April 2011
CMOS ANALOG AND MIXED SIGNAL DESIGN
(COMMON TO EMBEDDED SYSTEMS & VLSI DESIGN, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1) a) What is a cascade current mirror? Derive the output resistance for both the long channel and short channel
   b) Distinguish between Resistor MOSFET Divider and MOSFET only voltage divider with appropriate equations. [12]

2) a) Give the complete analysis of noise performance of a CS Amplifier with gate Drain load.
   b) Prove that for a voltage series feedback amplifier with R_s=0, A_{If}=A_I. Derive the equation for R_{if} and R_{of} considering the feedback. [12]

3) a) Explain how constant gain and stability is achieved in wide swing differential amplifier.
   b) Consider two sets of input voltages, where the first set of signals is v_1 =+50 μv and v_2 = -50 μv and the second set is v_1 =+1,050 μv and v_2 = 950 μv. If the CMRR is 100, calculate the difference in output voltage obtained for the two sets of input voltages. [12]

4) a) Explain how adaptive biasing reduces the power dissipation and increases the output drive capability.
   b) Explain the design of an analog multiplier using squaring circuits with necessary circuits and diagrams. [12]

5) a) Explain how the comparator is characterized by DC performance and transient response.
   b) Design a switch capacitor filter with the transfer function, which has a pole at 500 Hz and a zero at 5khz. The low frequency gain of the circuit is 20 dB. Use a lossy integrator. [12]

6) a) What is a Flash converter? Discuss the working of a 3-bit Flash A/D Converter.
   b) Design a 3-bit Flash ADC with quantization error centered about zero LSBs. Determine the worst case DNL and INL if resistor matching is known to be 5%. Assume V_{ref}=5v. [12]

7) a) Explain the design aspects of sample and hold circuits.
   b) Using stochastic approach, evaluate the average value of quantization error and hence deduce the signal to noise ratio for an ADC. [12]

8) Write a short notes on any **Two**
   a) Design procedure for CMOS differential amplifier.
   b) ADC architecture.
   c) Folded cascade amplifier. [12]

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